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Material Improvements and Device Processing on APIVT-Grown Poly-Si Thin Layers

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ABSTRACT

Means to develop efficient solar cells using as-deposited large-grain (~20 μm) atmospheric pressure iodine vapor transport (APIVT) thin-silicon materials are explored with grain boundary passivation and low-temperature device processing. Hot-wire chemical vapor deposition (HWCVD) a-SiN_x:H films are used as anti-reflection coating and passivation layers. After thermal annealing at various temperatures, V_{oc} of the solar cell devices was improved by about 10%, and J_{sc} was increased by as much as 46%. A HWCVD-deposited a(μc)-Si emitter reduces the open-circuit voltage loss caused by grain boundaries in the polycrystalline APIVT-Si layers. Epitaxial growth on metallurgical grade (MG) silicon seeded substrates results in very large grain sizes so that a much less stringent passivation process would be needed. With optimized growth conditions, we are able to eliminate gas-phase nucleation that leads to spurious growth in the bulk and on the surface of silicon films. A smoother surface and nearly isotropic growth characteristics are also obtained, compared to films grown earlier.

1. Introduction

Direct deposition of large-grain (~20 μm) polycrystalline-silicon thin layers has been achieved by atmospheric-pressure iodine vapor transport (APIVT) at moderate temperatures of about 900ºC on non-silicon substrates such as mullite, Corning LGA-139® glass-ceramics, or Carborundum Hi-Therm™ aluminum nitride ceramics. The average grain size obtained by APIVT is about ten times that achievable by a typical chlorosilane-CVD process at similar temperatures. However, development of efficient solar cells using these APIVT polycrystalline thin-silicon materials is still hampered by grain boundaries and lack of satisfactory processing techniques for junction formation. On one hand, simulations indicate that an effective grain-boundary passivation technique is still needed to attain a recombination velocity less than 10^4 cm/sec in order to keep open-circuit voltages above 550 mV. On the other hand, some available passivation techniques require either a high-temperature (>800ºC) step (e.g., H^+) or low temperatures (<300ºC) throughout the post processing (e.g., Li^+), which either causes impurity contaminations or is incompatible with conventional device processing. The research effort reported here will meet such challenges from three different directions to achieve efficient thin-Si solar cells.

Most of our earlier poly-Si films show spurious growth on the surface or in the bulk of the films, or anisotropic growth characteristics with very pronounced growth facets, leading to rough surfaces with steep cliffs and overhangs at grain boundaries. Such a surface morphology inevitably causes junction shunting and poor fill factors. Our material-improvement effort focuses on these issues.

2. Passivation

Hydrogen passivation is a common practice for device processing, usually accomplished with an anti-reflection a-SiN_x:H layer deposited by a (remote) plasma-enhanced chemical vapor deposition (PECVD) technique. It has only recently been demonstrated that HWCVD-deposited silicon nitride could be made with as much hydrogen as PECVD-deposited films and, consequently, have similarly effective passivation effects.

We deposited a-SiN_x:H films on diffused-junction solar cell devices of APIVT-grown polycrystalline silicon layers with a HWCVD technique. The filament was heated to 2100°C at a distance of 5 cm to the samples, and the resulting substrate temperature was about 250°C. A SiH_4:NH_3:H_2 flow ratio of 2:3:25 in sccm was used under a total pressure of 25 mTorr. A deposition rate of 2 Å/sec was obtained, and the resulting a-SiN_x:H films have an index of refraction between 2.11 and 2.15. These films have been measured by FTIR from the Si-H stretch mode at 2100 cm^{-1} to have (2-11)x10^{21} cm^{-3} of hydrogen. After thermal annealing at various temperatures, V_{oc} of the solar cell devices was improved by about 10%, and J_{sc} was increased by as much as 46%. However, the absolute values of V_{oc} are still just below 0.50 V, so passivation needs to be even more effective, for example, by incorporating more hydrogen in the silicon nitride film. The improvements are generally larger after higher-temperature anneals up to 500ºC. Annealing at temperatures higher than 500ºC led to fewer enhancements, possibly due to impurity contamination from the substrates and a loss of hydrogen. We have also demonstrated a 50% increase in Hall mobility by hot-wire cracking of molecular hydrogen.

3. Low-Temperature Junction Formation

In depositing thin poly-Si layers on low-cost substrates, a deposition rate of >3 μm/min is enough to have minimal impurity diffusions from the substrate except for Ni and Fe, which are tolerable to their solubility limit in silicon at 900ºC. The normal high-temperature process for junction diffusion could cause undesirable contamination by other more detrimental elements such as Mo and W. Furthermore, due to energy band bending caused by Fermi-energy pinning at grain boundaries, the built-in voltage of the p/n junction will be reduced on both sides of a diffused junction or a grown-in junction formed during poly-Si layer deposition. Therefore, using thin-film a(μc)-Si as the emitter to form a junction with the APIVT-deposited poly-Si thin layer is advantageous because of low temperature (~250°C) and elimination of grain boundaries on one side of

the junction. A herojunction with an intrinsic thin layer (HIT) structure is normally accomplished by PECVD, but we use the HWCVD technique to fabricate the devices. The advantages of HWCVD over PECVD are less interface damage due to absence of a plasma, in-situ atomic hydrogen treatment to passivate defects or surface cleaning before deposition, and fast deposition rate. Such a device made on an APIVT-deposited poly-Si layer with a metal grid and an indium tin oxide (ITO) layer exhibits V_{oc} = 0.48 V without passivation, compared to V_{oc} = 0.42 V for a diffused-junction cell made on a similar material.

The HIT solar cell structure is shown in Fig. 1. The n-type emitter consists of a 50-Å intrinsic a-Si buffer layer with a heavily phosphorous-doped microcrystalline silicon dead layer of 80 Å. Our best demonstration HIT device made on a CZ-Si substrate shows a conversion efficiency of 13.3%, as shown in Fig. 2, which compares favorably with our standard diffused junction (875°C) devices on CZ c-Si with double AR coating and a conversion efficiency of 14.1%. The stability of the HIT device is very good with only 3% degradation in efficiency after standard AM1.5 light-soaking for 600 hours at 50°C in air, which could be caused by B-O complexes in the CZ-Si substrate instead of the emitter.

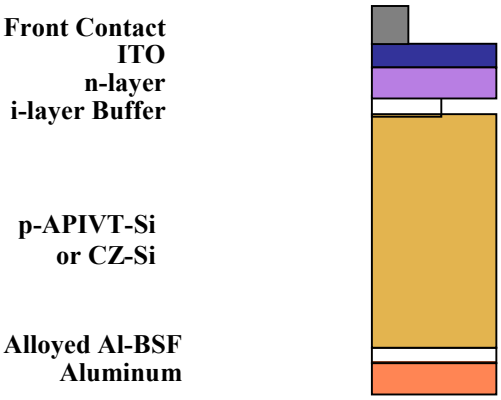

Figure 1. Schematic of a HIT device.

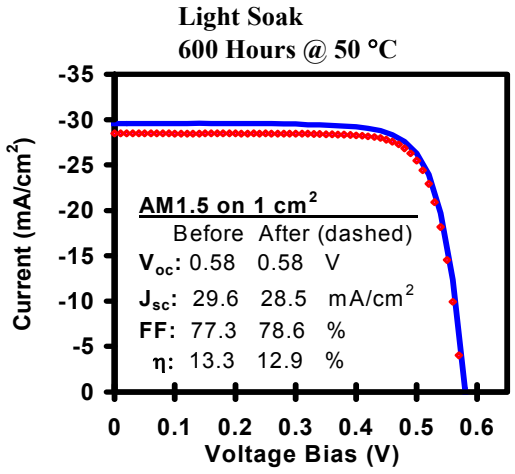

Figure 2. IV Curves for a HIT device on CZ-Si before and after light soaking.

A typical IV curve of such a low-temperature junction device on an APIVT poly-Si film is shown in Fig. 3. Apart from a still-low V_{oc}, the fill factor is also very poor due to a discontinuous ITO caused by the rough surface.

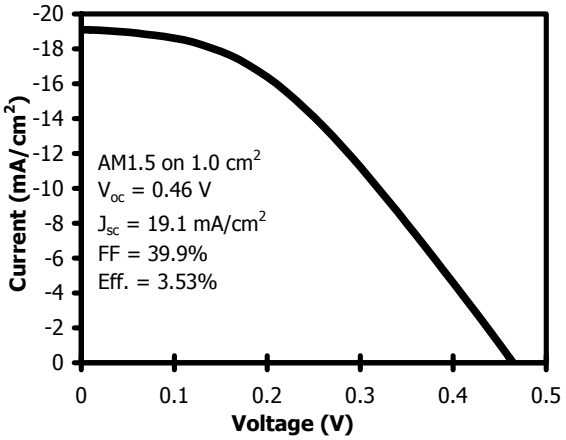

Figure 3. IV curve of a HIT device on APIVT-grown poly-Si thin film (~20 μm thick).

4. Elimination of Spurious Growth

The spurious growth of silicon particles could either leave pockets of very low-quality silicon buried in the bulk of a silicon film, or on the surface of a silicon layer, as shown in Fig. 4, which causes a lot of difficulties for device processing or forms low-quality junctions. Reducing the source-silicon temperature from 1350° to 1150°C has consistently prevented particle formation.

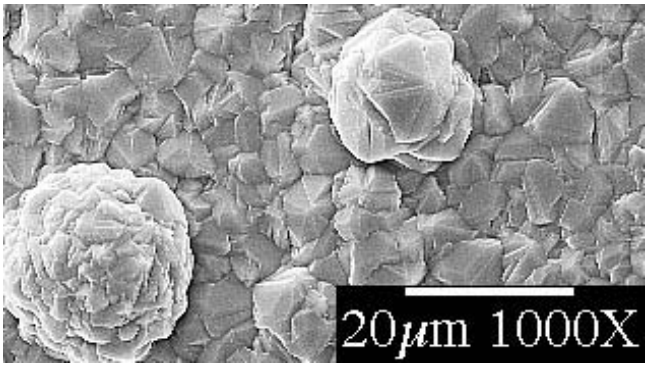

Figure 4. A typical spurious growth on the film surface.

These results confirm our earlier belief that these particles are attributable to gas phase nucleation due to excessive free-energy driving force. According to partial pressures of SiI_2 and SiI_4 as functions of temperature as calculated by Wajda and Glang [2], as one decreases the source temperature from 1350° to 1150°C while maintaining the same substrate temperature at 950°C, the partial pressure of SiI_4 at the source location is significantly increased and the partial pressure of SiI_2 is slightly reduced. Both factors lead to a decreased free-energy driving force and slowed silicon mass transport, and therefore complete elimination of gas-phase particle formation is possible.

We have not observed any noticeable drop in film growth rate (~1 μm/min) even with the lower source temperature,

possibly because of reduced silicon particle formation normally lost to the reactor wall anyway.

5. Smoother Surface and More Conformal Grain Boundaries

Most of our earlier poly-Si films were deposited at a substrate temperature of 800°-850°C, in an attempt to minimizing substrate contamination. However, these films generally show anisotropic growth characteristics with very pronounced growth facets, leading to rough surfaces with steep cliffs and overhangs at grain boundaries. Such a surface morphology inevitably causes junction shunting and poor fill factors. With higher substrate temperatures of >950°C, the surface morphology improved dramatically, as shown in Fig. 5. The growth is now more isotropic with much less faceting, so the surface is much smoother and the grain boundaries are more conformal.

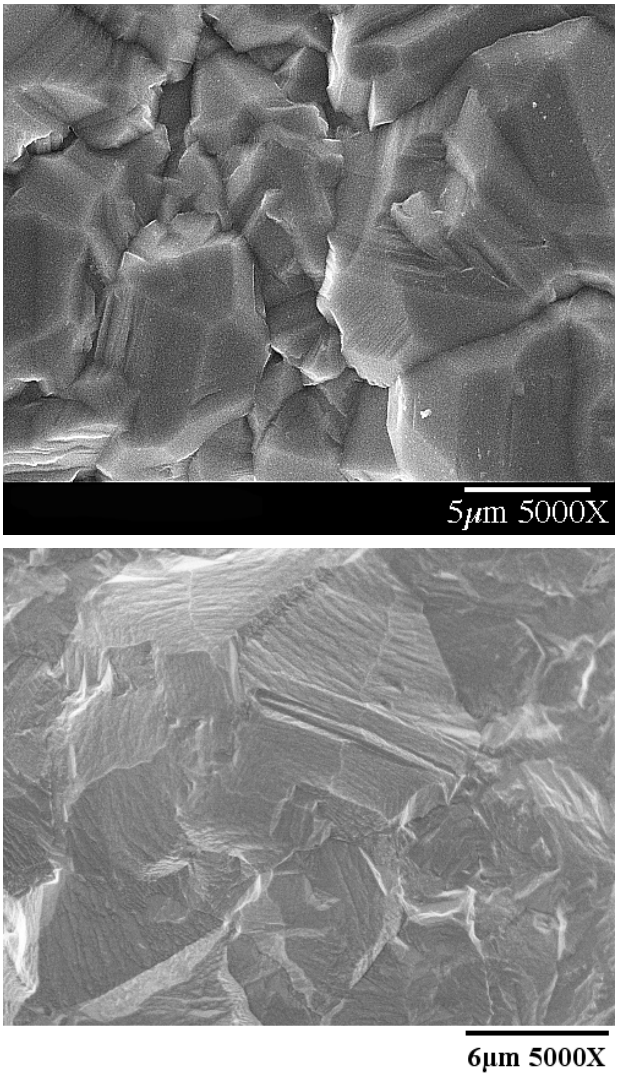

Figure 5. Anisotropic growth at 850°C (top) and nearly isotropic growth at 950°C (bottom).

6. Summary

The HWCVD technique has been used to develop and improve APIVT thin-Si PV devices by depositing μc-Si emitters for heterojunction formation; by depositing a-SiN_x:H films for antireflection coatings and defect passivation; and by cracking molecular hydrogen for defect passivation. Photovoltaic devices with a HWCVD μc-Si emitter on APIVT epitaxial silicon exhibit greater than 8% efficiency, similar to those made with diffused junctions. On poly-Si APIVT layers, a HWCVD-deposited μc-Si emitter reduces open-circuit voltage loss caused by grain boundaries. HWCVD a-SiN_x:H films improve minority-carrier lifetimes significantly after annealing at temperatures up to 500°C. Hot-wire hydrogenation improves Hall mobility by about 50%. Further development and optimization of HWCVD in junction formation and passivation is needed to improve poly-Si APIVT thin-layer solar cells.

With optimized growth conditions, we are able to eliminate gas-phase nucleation that leads to spurious growth in the bulk and on the surface of silicon films. A smoother surface and nearly isotropic growth characteristics are also obtained, compared to films grown earlier.

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REFERENCES

[1] T.H. Wang and T.F. Ciszek, "Growth of Large-Grain Silicon Layers by Atmospheric Iodine Vapor Transport," *J. Electrochem. Society*, **147** (5) (2000) 1945-1949.

[2] R. Glang and E.S. Wajda, "Silicon" in *The Art and Science of Growing Crystals*, Ed. J.J. Gilman, John Wiley & Sons, New York, (1963) 80-92.

[3] Qi Wang, Matt Page, Yueqin Xu, Eugene Iwaniczko, Evan Williams, Tihu Wang and Ted Ciszek, "Development of Hot-Wire CVD n-type Emitter on p-type Crystalline Si Based Solar Cells", Extended Abstract of 2nd International Conference on Cat-CVD (Hot-Wire CVD) Process, NREL/CP-520-30476, September 2002, Denver, Colorado. To be published by *Thin Solid Films*.

[4] T.H. Wang, Q. Wang, M.R. Page, R.E. Bauer, and T.F. Ciszek, "Hydrogen Passivation and Junction Formation on APIVT-Deposited Thin-Layer Silicon by Hot-Wire CVD," Extended Abstract of 2nd International Conference on Cat-CVD (Hot-Wire CVD) Process, NREL/CP-520-30476, September 2002, Denver, Colorado. To be published by *Thin Solid Films.*

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